# Introduction

The purpose of the design described here is to provide bias and control voltages for the PHYS 439 lab course Alpha experiment.

# Features

## Arduino Interface

The design is in the form of an Arduino Mega shield, with the double-row connector removed. It should be compatible with the Mega, the Due, and the Uno.

The functionality described is effectively doubled: two DC bias outputs are provided, two 0-20VDC control voltages, and two relay control pins.

## Bias outputs

The design includes two ISEG DC/DC high voltage modules. Modules in this series have output voltages ranging from ±200V to ±1kV (polarity chosen when ordering). The design is made to work with the ±200V module (AP002255p05 or AP002255n05). **Trace clearance should be adequate for ±200V but may not be for 1kV – modifications or design changes may be needed to ensure no breakdown occurs.**

Note that for current PHYS 439 requirements, only one bias output is required per setup. The second one is provided for possible future use in other circumstances.

The bias output voltage is controlled by Arduino outputs, via a 0-2.5V control signal. The two available DAC output pins of the Due are supported, as are a couple of PWM pins that can be controlled by the Mega or Uno.

In order to accommodate usage with PWM outputs from Mega or Uno with minimal PWM ripple appearing on the output, a third (or possibly fourth) order lowpass filter is included.

A footprint for a Zener diode is provided on each bias output, as well as a series resistor. This allows hard limiting of the output voltage.

## Bias Voltage Readback

The ISEG DC/DC module provides a voltage readback signal, which is connected to an analog (ADC) input pin on the Arduino.

## Proportional Voltage Outputs

Outputs 0 - ~20V, proportional to PWM or analog output.

# Circuit Details

## Analog Channels

There are a total of four analog channels, arranged in two identical groups. Each group consists of the first channel, which supplies a control voltage to an ISEG DC/DC module, and a second channel, which controls a control voltage output output by an op amp on a header pin. Each analog channel implements a lowpass filter, allowing a PWM signal to be converted to a smooth analog voltage.

### Lowpass Filter

The lowpass filters, contained in the double\_lpf circuit block in the schematic, each consist of a passive RC lowpass filter followed by an op amp buffer and an active Sallen-Key (double pole) lowpass filter. For the sake of component references, discussion pertains to the top filter in the top circuit block.

The same filter circuit is used, though configured differently in each case, for the bias voltage control (particularly if a PWM control is used), and also for the 0-20V proportional valve control voltage. In each double\_lpf block, the top filter controls an ISEG bias voltage module, while the bottom filter provides the 0-20V output.

Note that a filter is not necessary if a DAC output is used for the bias voltage setting. In this case, the second state can be configured as a voltage follower (unity gain) amplifier, and the first stage can be configured as an attenuator using the input resistor (outside the block) and R9.

Component values are determined based on the amount of DC gain (or attenuation) required, as well as the desired filter response (settling) time, on the PWM frequency (if applicable), and the amount of acceptable PWM frequency ripple on the output. The following design principles should be followed.

### First-Stage Attenuator and Filter Design

The first stage consists of an attenuator and a buffer. The buffer may have gain, and if the feedback capacitor is populated, it may also include frequency rolloff, but only down to unity gain. Since it cannot function as a very effective filter, the feedback capacitor is not populated.

The design can accommodate a 3.3V or 5.0V PWM, with component changes.

#### Frequency Response

This filter is configured differently depending on the usage. In both cases, we aim for ωC ≈ 10s‑1. Again we use C=1µF. The effective R is 100kΩ // 220kΩ for the first channel, and 100kΩ for the second.

#### ISEG module control

For PWM = 5.0V, we need an overall DC gain of 0.5, to take the maximum average PWM voltage 5V to 2.5V (the maximum input level for the ISEG control voltage). The DC gain of the Sallen-Key filter is fixed at 1.6. Therefore we need an attenuation of 1/3.2. We choose R9 = 100kΩ, and the input resistor R1=220kΩ.

For 5.0V input, the feedback resistor R13 is set to 1kΩ, and R11 is not populated.

For 3.3V input, we need to boost the signal, so we populate R11 = 2.7kΩ, giving us a gain of 1+1/2.7 = 1.37 ≈ 5.0 / 3.3. **Note that this does not give the full range: on a 200V ISEG module, the top output voltage will be approximately 180V.**

Note also that in order to provide a low enough voltage when the setting is put to zero, it’s necessary to place a 100Ω resistor across D2, to sink current from the ISEG module, which has a 10kΩ pullup to 5V. When 100Ω is added in this way, the output voltage can be set under 2V.

A transient of up to ±7V (depending on the ISEG module polarity) is produced when the 5V supply is connected.

#### Proportional Valve Control

We need an overall DC gain of 4, to take a full scale 5.0V PWM signal to 20V (the maximum input level for the proportional valve control input). The DC gain of the Sallen-Key filter is fixed at 1.6. Therefore we need an gain of 2.47. We choose R4 = 100kΩ, we don’t populate R10, and we choose R12=1kΩ and R14=1.5kΩ.

For use with a 3.3V signal, we change R12 to 470Ω, increasing the gain to 4.19.

### Second-stage Gain Setting

The gain of the second state relates to the Q of the second stage as follows:

For Q=0.5, the amplifier can be configured as unity gain. However, the frequency response sags quite a bit in the passband and so a Q of 0.707 (A ~1.6, critically damped) to 1 (A = 2, a bit of peaking) may be preferable. We will choose A=1.6. Note that this affects the filter’s DC gain. This determines the values of R19 and R21 as follows:

To achieve the specified gain, we choose R21 = 680, R19 = 1.1kΩ, for a nominal G = 1.618

### Second-Stage Sallen-Key Filter Design (frequency response)

For more details on Sallen-Key filter design, see e.g. Don Lancaster, Active-Filter Cookbook, <http://read.pudn.com/downloads470/ebook/1971235/Active-Filter%20Cookbook(D.Lancaster).pdf> .

We will use equal-value C and R, noting that for the normalized case ω = 1, R=C=1.

Choosing R=100kΩ and C=1µF, we have ωC = 1 / RC = 10s-1, so fC=ωC / 2π = 1.6Hz

### Overall DC Gain Calculation

The following DC gain values are used in the firmware to compute the PWM or DAC counts to be used in setting analog outputs.

|  |  |  |
| --- | --- | --- |
| **Parameter** | **Bias** | **Valve** |
| Rin | 220k | 100k |
| Ring | 100k | Open |
| atten=Ring/(Ring+Rin) | 0.3125 | 1 |
| Rf1 | 1k | 1.5k |
| Rg1 | 2.7k | 470 |
| G1 = 1+Rf1/Rg1 | 1.3704 | 4.1915 |
| Rf2 | 680 | 680 |
| Rg2 | 1.1k | 1.1k |
| G2 = 1+Rf2/Rg2 | 1.6182 | 1.6182 |
| **Total = atten\*G1\*G2** | **0.69299** | **6.783** |

## Bias Output Connection

The ISEG modules M1/M2 are coupled to output connectors J1/J3 via resistors R43/R44. Zeners D6/D7 can be put in place to limit the voltage. Note that the orientation of the Zener must be changed if a negative voltage module is used. If a Zener is used, R43/R44 must be small enough so that any Zener leakage current causes negligible voltage drop. A value of 10kΩ is recommended.

The experiment may require the use of a large resistance (over 1MΩ), in series with the detector being biased. This resistance could be provided by R43/R44, but as per the warning above, if a Zener is used, it may be necessary to provide the large series resistance as a leaded part, connected to J1/J3.

## Analog Sense Channels

The ISEC DC/DC module includes an analog read-back signal that can be used to determine the actual output voltage.

A connection is made (via a resistor) from each ISEG module analog read-back pin, to an Arduino analog input.

## Relay Channels

There are four relay channels, shown in the schematic as having two channels in each group. Each channel simply consists of a connection from an Arduino digital pin, to a pin on header J5/J6.

Note that for convenience in accessing pins and avoiding interference with the bias and valve control headers, the second group’s channels are used as RELAY1 and RELAY2.

# Arduino and Firmware Pin Mapping

This table outlines the Arduino and shield resource usage, and the addressing of each function with the current firmware. Notes:

Implemented or default options are shown in bold

Depopulated channels are shown in italics

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Firmware function** | **Group / channel** | **JP to connect or R to populate)** | **Arduino Pin** | **Shield output pin** |
| BIAS1 | G1 / CH1 | **R1** / R2 | **5** / DAC0 (A12) | J1-1 |
| VALVE1 | G1 / CH2 | R3 / **R4** | 5 / **9** | J2-2 |
| *BIAS2* | *G2 / CH1* | *R5 / R6* | *6 / DAC1 (A13)* | *J3-1* |
| *VALVE2* | *G2 / CH2* | *R7 / R8* | *6 / 10* | *J4-2* |
| Not implemented | G1 / CH1 | JP1 **(1-2)** / (2-3) | **14** / 3 | J5-1 |
| Not implemented | G1 / CH2 | JP2 **(1-2)** / (2-3) | **15** / 2 | J5-5 |
| RELAY1 | G2 / CH1 | JP3 **(1-2)** / (2-3) | **20** / 3 | J6-1 |
| RELAY2 | G2 / CH2 | JP4 **(1-2)** / (2-3) | **21** / 2 | J6-5 |
| BIAS1 SENSE | G1 / CH1 | R37 | A0 | n/a |
| BIAS2 SENSE | G2 / CH1 | R38 | A1 | n/a |

# Connection to External Relay Module

The shield is designed for connection to an external relay module. It has been tested with “Sunfounder 2 Channel Relay” (available from Amazon), as shown in below (photograph and schematic). The connection to this module is made as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Shield** | **Relay board** | **Note** |
| RELAY1 | J6-1 | IN1 | Active low |
| RELAY2 | J6-5 | IN2 | Active low |
| VCC | J6-3 | VCC | +5V, see discussion |
| GND | J6-2 | GND |  |

## Note on 3.3V / 5.0V interface

The relay module is designed to take an active-low signal to turn on the relay. For this reason, in the firmware, the “ON” condition writes a zero to the relay pin. If the shield is to be used with a relay module that requires an active high signal, the firmware should be modified.

Note that +5V is supplied from the shield to the relay module, regardless of whether the Arduino board is 5V (AtMega2560) or 3.3V (Due). When used with a 3.3V board (the Due), the situation requires some care to be taken, since the current return path from the +5V VCC pin passes through the 3.3V I/O pin. The condition causing potential concern is when the output is off (high). In this condition, the 3.3V I/O pin is being pulled high by current from the 5V rail, requiring any leakage current to be sunk by the pin’s ESD diode.

The current path in question includes a 1kΩ resistor in series with two LEDs (one inside the optoisolator, another serving as an indicator). Each LED likely has a nominal forward voltage >1V. Measuring the open input pin with a multimeter (10MΩ to GND) we only read around 2.7V. Therefore, the leakage current into a 3.3V pin will be quite small. The only thing to watch for, would be any effect on the analog read-back, which might be sensitive to injection of current into the ESD diodes.

If this ever were to be a concern, it could be resolved by removing the jumper between RY-VCC and VCC (shown as green in the photo), connecting RY-VCC to 5.0V, and connecting VCC to 3.3V (which requires adding a pin to the shield).

## Relay Module



